JC873 U.S. PTO 10/077258 02/14/02

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U.S. UTILITY Patent Application

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10077258	02/14/2002	257	324	2814	

**APPLICANTS: Mo Brian; Chau Duc; yl

**CONTINUING DATA VERIFIED: yes

THIS APPLICATION IS A DIV OF 09/286,168 04/05/1999 yl

** FOREIGN APPLICATIONS VERIFIED: None yl

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐

Foreign priority claimed	☐ yes ☑ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☑ no	018865-001010US
Verified and Acknowledged Examiners's intials	yl	

TITLE : Method of forming a trench transistor having a superior gate dielectric

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED	
		Total Claims: 10	Print Claim for O.G: 1
ISSUE FEE		DRAWING	
Amount Due / Date Paid		Sheets Drwg.: 5	Figs.Drwg.: 7 / Print Fig.: 3, 4
☐ TERMINAL DISCLAIMER	Primary Examiner	Application Examiner	
	PREPARED FOR ISSUE		

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